

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A testing device of a semiconductor integrated circuit having more than one different logics and JTAG circuits built in, which executes an in-circuit test of said logics, wherein;

the JTAG circuit includes a boundary scan register that executes a test of said logic in accordance with a test data input and stores a test result; a data register; a ~~pseudo-bypass~~ transfer register having a bypassing function of said test data input; a first selector connected to said data register and said ~~pseudo-bypass~~ transfer register, which selectively takes out outputs of said registers, wherein said data register is configured for selecting an output of said transfer register by controlling said first selector when said more than one different logics are simultaneously set to be in a test mode; a bypass register having a bypassing function of said test data input; an instruction register for giving an operation command; and a second selector that is connected to said boundary scan register, said first selector, said bypass register, and said instruction register, which is selectively controlled by said instruction register, and

the JTAG circuits are provided to each of said logics, and the output from said second selector of a specific logic is an input of another logic.

2. (Cancelled)

3. (Currently Amended) [[A]] The testing device of a semiconductor integrated circuit according to claim 1, wherein said ~~pseudo-bypass~~ transfer register has the same configuration as that of said bypass register.

4. (Currently Amended) [[A]] The testing device of a semiconductor integrated circuit according to claim 1, wherein said ~~pseudo-bypass~~ transfer register has a selector provided on the input thereof[[, whereby]] such that the test data input to be bypassed and arbitrary information ~~can be~~ are inputted selectively.

5. (Currently Amended) [[A]] The testing device of a semiconductor integrated circuit according to claim 1, wherein said ~~pseudo-bypass~~ transfer register is configured with plural bits[[, whereby]] such that the test data input to be bypassed through the selector and arbitrary information ~~can be~~ are inputted selectively by each bit.

6. (Currently Amended) A testing device of a semiconductor integrated circuit having more than one different logics and JTAG circuits built in, which executes an in-circuit test of said logics, wherein:

each of said logics is provided with: a control block including a boundary scan register that executes a test of said logic in accordance with a test data input and stores a test result, a data register, a ~~pseudo-bypass~~ transfer register having a bypassing function of said test data input, and a first selector connected to each of said registers, which selectively takes out outputs of said registers, wherein said data register is configured for selecting an output of said transfer register by controlling said first selector when said more than one different

logics are simultaneously set to be in a test mode; and a bypass register; an instruction register; and a second selector that is connected to ~~these registers and~~ said bypass register, instruction register and first selector, which is selectively controlled by said instruction register, and

the output from the second selector of a specific logic is an input of another logic.

7. (Currently Amended) A testing device of a semiconductor integrated circuit having more than one different logics and JTAG circuits built in, which executes an in-circuit test of said logics, wherein:

each of said logics is provided with: a control block including a boundary scan register that executes a test of said logic in accordance with a test data input and stores a test result, a data register, a ~~pseudo-bypass~~ transfer register having a bypassing function of said test data input, and a first selector connected to each of said registers, which selectively takes out outputs of said registers, wherein said data register is configured for selecting an output of said transfer register by controlling said first selector when said more than one different logics are simultaneously set to be in a test mode; a bypass register and an instruction register that are common to each of said control blocks; and a second selector connected to said each control block, said bypass register and said instruction register, which is selectively controlled by the instruction register, and

the output from the first selector of a specific control block is an input of another control block.

8. (Currently Amended) A test method of a semiconductor integrated circuit, which carries out an in-circuit test thereof by a testing device thereof, according to any one of claims 1 and 3 to 7 ~~claims 1 to 7~~.